The Impact of Aging on the Radiation Robustness of Combinational Cells

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***Abstract*—This study investigates the impact of aging degradation on the performance of standard logic cells through simulations. The results show that aging affects the high-to-low (HL) and low-to-high (LH) transition times of logic gates, with simpler gates experiencing more aging than their counterparts with more inputs. Furthermore, more complex gates exhibit greater variability in degradation, particularly in HL transitions. The analysis also reveals that considering both Bias Temperature Instability (BTI) and Single Event Transient (SET) effects is crucial for designing reliable digital circuits. The comparison of BTI with SET effects relative to the fresh state highlights the significant impact of cell degradation on the robustness of logic gates.**

***Index Terms*—Circuit simulation, combinational circuits, logic cells, radiation effect, BTI, SET, robustness, aging**

I. Introduction

The integrated circuit fabrication technology is in constant miniaturization. This persistent reduction in feature size enables the continuous evolution of integrated systems, leading to increased performance, efficiency, and functionality. However, this trend towards smaller dimensions introduces several adverse effects. One significant issue is the aging of semiconductor devices, as the smaller geometries tend to exacerbate wear-out mechanisms such as Bias Temperature Instability, electromigration, and time-dependent dielectric breakdown. Additionally, the reduced feature sizes diminish the robustness of these circuits against radiation effects [1]. With lower radiation tolerance, integrated circuits become more susceptible to soft errors caused by cosmic rays and other radiation sources, which can induce transient faults, data corruption, or permanent damage [2]. Consequently, while miniaturization propels technological progress, it also necessitates new strategies for ensuring reliability and longevity in advanced electronic systems.

II. Background

The Bias Temperature Instability (BTI) leads to the aging of MOSFET transistors, resulting in a gradual and progressive increase in the threshold voltage (Vth), which affects the behavior of the transistors within an integrated circuit (IC) [3]. There are two types of BTI: Negative BTI (NBTI), which occurs in PMOS devices, and Positive BTI (PBTI), which occurs in NMOS devices. Both types occur due to the stress experienced by the transistors while conducting, whereas during their non-conducting periods, they undergo a recovery phase. The BTI effect comprises two phases: stress, when the transistor is conducting, and recovery. However, the transistor cannot fully recover its threshold voltage, leading to a gradual degradation in performance over time [4].

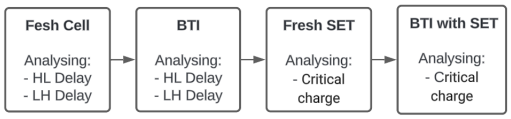

Fig. 1. Flowchart about the simulation.

Furthermore, electronic devices used in space applications face a significant possibility of experiencing undesirable effects caused by cosmic rays and radiation. These circuits, predominantly employed in satellites for various purposes such as communication, remote sensing, research, military objectives, among others [2]. The energetic particle can collide with electrons inside the transistor, creating electron-hole pairs and generating charge along the particle's path. A frequently employed approach to model the waveform of the induced current in a Single Event Transient (SET) is the use of the double exponential function. This waveform is widely used in transient simulations [5]).

The response time of ICs can be similar to the time required to collect charge from a single event, dynamically interacting with the circuit's output. Therefore, it is crucial to accurately model the shape of the transient pulse and analyze potential soft errors [5][2]. It is essential to consider circuit characteristics, such as the impact of charge collection, in the generation and propagation of single event transients (SETs) within the IC [6][5][2].

III. Methodology

This work utilizes the ASAP7 technology for evaluation, as described in [7]. Transistors with a gate length of 20nm and two fins each were simulated using the open-source Sandia circuit simulator Xyce™ [8], which offers compatibility with the chosen technology. To assess circuit robustness, simulations incorporated aging and soft error effects. Initially, the following standard cells were chosen, Figure 2, for evaluation: inverter, NAND2, NAND3, NOR2, NOR3, AOI21a, AOI21b,

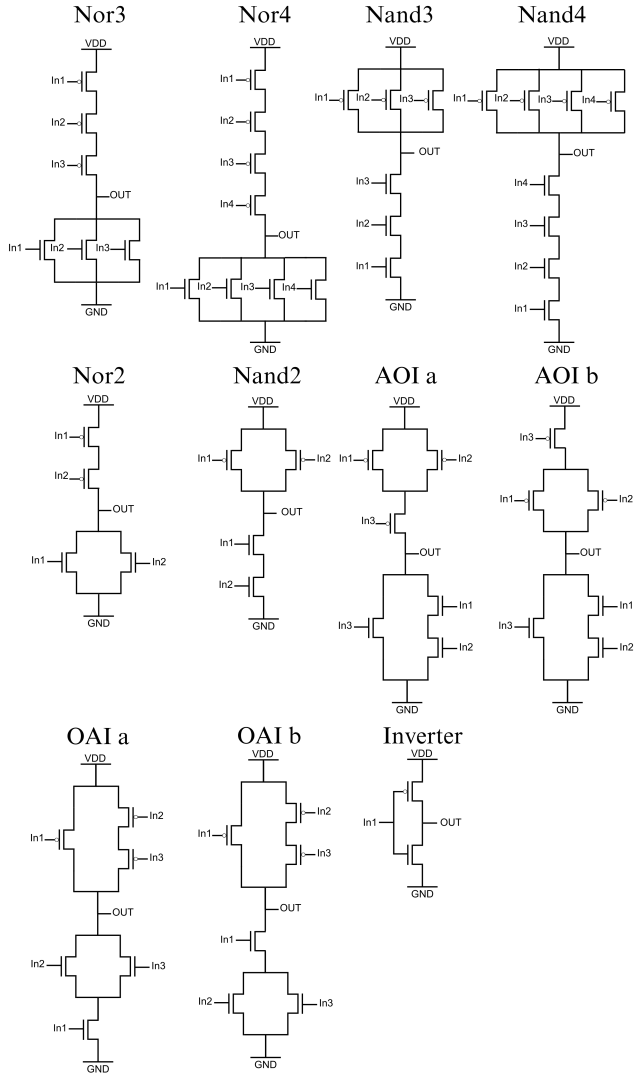

Fig. 2. Standard cells tested.

OAI21a, and OAI21b. The circuits were powered with a supply voltage of 0.7V. All test results are available on GitHub [9].

The evaluation flow presented in Figure 1 includes: (1) Fresh Cell, (2) BTI analysis, which examines High to Low (HL) and Low to High (LH) delays, (3) Fresh SET, and (4) BTI with SET, where the critical charge of the logic gate is assessed. This approach allows for a systematic evaluation of standard cell behavior under realistic operating conditions.

A. Fresh Cells

After constructing the cells, tests were conducted to measure the timing of each logic gate, both for HL and LH transitions. All logic gates were tested using the characteristics mentioned earlier.

B. BTI model

The BTI phenomenon impacting the threshold value (V_{th}) on both transistors. To perform the analysis of the aging of logic blocks, it is necessary to simulate the effects of NBTI and PBTI. With this in mind, a model was adopted that reproduce the threshold voltage degradation. The electrical model that represents the effects of aging is based on the inclusion of a voltage source in the gate of pMOS and nMOS transistors [10]. Furthermore, the degradation values in each transistor were defined according to the probability of the transistor being under degradation bias.

TABLE I
AGING VOLTAGE (V_{aging}) IN RELATION TO TSP FRACTION.

TSP	V_{aging} (mV)	TSP	V_{aging} (mV)
1	50	3/8	42.5
3/4	47.7	1/4	39.7
1/2	44.5	1/8	35.4

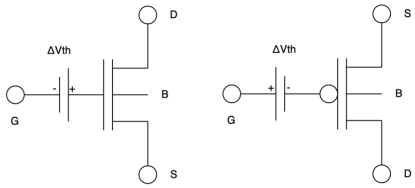

Fig. 3. nMOS and pMOS with aging model.

$$\Delta V_{th} = A.(TSP.t)^n \tag{1}$$

The parameters used were: *A*, a technology-dependent constant set at 3.9 x 10^{-3}; *n*, the exponential time constant of NBTI set at 1/6; *t*, representing time; and the Transistor Stress Probability (TSP) value for each transistor [11][6]. Additionally, a voltage value of 50mV (V_{th}) was employed, corresponding to a TSP equal to 1 [12]. Consequently, it is possible to generate the voltage equivalence table (Table I) in relation to TSP. First, the time required to reach 50mV must be determined. Subsequently, this time and the other constants can be used to find the voltage value for each TSP [6].

With the TSP values determined for each input of every logic gate, a voltage source corresponding to these TSP values was applied to the transistor's gate [10], as depicted in Figure 3. The voltage value applied to the transistor gate is determined by the values listed in Table I, which vary depending on the TSP of each input and logic gate. By applying voltage sources to the transistors within a cell, the High to Low (HL) and Low to High (LH) transition times of the logic gate for each input were analyzed and compared with its fresh model.

C. TSP

The Transistor Stress Probability (TSP) is a metric used to evaluate the likelihood of a transistor operating under stress conditions throughout its lifespan. To calculate the TSP, it is essential to understand the operating conditions of the transistor within a specific circuit, including voltage, current, and temperature.

In the TSP approach, degradation is assessed by considering the voltage bias between the gate terminal and the source and drain terminals. Furthermore, the TSP is defined as the

probability of a PMOS/NMOS transistor being negatively or positively biased. This probability depends on several factors: it depends on the signal probabilities of circuit inputs, usually defined as the probability of a node to be at high value (logic 1); and the position of the transistor within the circuit [13]. Using the results from these simulations, it is possible to construct a probability distribution curve that reflects the cumulative probability of stress over time.

The table II exemplifies the result of the TSP calculation for an OAI21-V1 logic gate, where equal probabilities were considered for the inputs A, B, and C of the logic gate. Thus, it was possible to calculate the probability of each of the transistors constituting the circuit being stressed in the occurrence of each input vector, as well as the total probability of each of them being stressed considering all possible input vectors.

TABLE II
OAI21 (VERSION 1) ANALYSIS

A	B	C	P1	P2	P3	N1	N2	N3
0	0	0	stress	stress	stress	-	-	-
0	0	1	stress	stress	-	-	-	-
0	1	0	stress	-	stress	-	-	-
0	1	1	stress	-	-	-	-	-
1	0	0	-	stress	stress	-	-	stress
1	0	1	-	stress	-	-	stress	stress
1	1	0	-	-	-	stress	-	stress
1	1	1	-	-	-	stress	stress	stress
stress prob.			0.5	0.5	0.375	0.25	0.25	0.5

D. SET model

To simulate the SET, it is necessary to add a double exponential current source to the circuit according to Equation 2. To add the current source requires the determination of four parameters: IPeak, $(t_{d2} - t_{d1})$, τ_1 and τ_2. The closest values found were based on the parameters of 90nm technology. For the short-term current source, $(t_{d2} - t_{d1})$ = 15 ps, τ_1 = 2 ps and τ_2 = 4 ps [5]. The IPeak value is adjusted to obtain a signal transition at the output.

$$\text{EXP}(I1\ I2\ td1\ \tau_1\ td2\ \tau_2) \tag{2}$$

For this article, $I1$ was set to zero and $I2$ was set to the minimum value required for a SET to occur at the output of the circuit, which is the IPeak of Equation 2. The times $td1$ and $td2$ differ by 15 ps. To generate a SET, the signal excursion must be equal to or greater than 50% of the supply voltage.

E. BTI + SET model

To analyze BTI and SET on the same logic gate, both models were added to the same cell to be studied. In other words, a voltage source was added at the input of each gate, according to the respective value of its TSP, and a double exponential at the gate output.

IV. ANALYSIS AND DISCUSSION

Initially, the circuit's behavior in its fresh state was analyzed to observe changes compared to the aging model. Subsequently, Bias Temperature Instability (BTI) tests were conducted as described in the methodology. The percentage of degradation of the aged cell relative to the fresh cell was calculated, as shown in Equation 3, for both phenomena. In Equation 3, D represents the percentage value of cell degradation. The analysis included the maximum, minimum, mean, and standard deviation of the percentage relative to the same fresh cell. The results for the BTI analysis are presented in Table III, which displays the data for the cells during HL and LH transitions.

$$\text{D} = 1 - \frac{\text{BTI}}{\text{Fresh Cell}} \quad \text{and} \quad \text{D} = 1 - \frac{\text{BTI with SET}}{\text{Fresh SET}} \tag{3}$$

A. Aging Degradation Analysis

The results reveal that NAND and NOR gates with fewer inputs experienced more aging compared to their four-input counterparts due to having a higher Transistor Stress Probability (TSP) in the transistor arrangement. This indicates that aging affects the HL and LH transition times of the cells.

TABLE III
EFFECTS OF AGING ON HIGH-TO-LOW AND LOW-TO-HIGH TRANSITION TIMES.

		Maximum	Minimum	Mean	S. Deviation
Inverter	HL	-	-	31.62%	-
	LH	-	-	20.58%	-
NAND-2	HL	24.88%	18.43%	21.65%	4.56%
	LH	20.30%	16.00%	18.15%	3.04%
NAND-3	HL	18.03%	16.20%	17.47%	0.94%
	LH	18.42%	13.56%	15.22%	2.47%
NAND-4	HL	15.84%	11.77%	13.63%	1.78%
	LH	16.60%	12.01%	13.30%	2.04%
NOR-2	HL	27.05%	21.07%	24.06%	4.23%
	LH	19.31%	16.95%	18.13%	1.67%
NOR-3	HL	23.56%	18.51%	19.13%	2.75%
	LH	14.91%	12.49%	14.12%	1.23%
NOR-4	HL	21.18%	16.97%	17.58%	1.92%
	LH	12.72%	7.75%	12.46%	2.40%
AOI-V1	HL	44.40%	27.02%	42.25%	9.47%
	LH	19.70%	14.37%	16.15%	2.71%
AOI-V2	HL	53.18%	19.32%	43.09%	17.39%
	LH	30.17%	10.32%	18.98%	9.95%
OAI-V1	HL	18.17%	14.04%	16.77%	2.10%
	LH	19.32%	12.21%	15.64%	3.56%
OAI-V2	HL	24.19%	14.74%	19.35%	4.73%
	LH	15.29%	10.86%	14.23%	2.31%

Moreover, simpler logic gates like inverters, NAND, and NOR gates exhibit higher degradation in HL transitions than in LH transitions. Conversely, more complex gates like AOI-V1 and AOI-V2 display greater variability in degradation, particularly in HL transitions.

The AOI-V2 gate exhibited the largest difference in HL transition time and the highest LH transition time. Additionally, the AOI-V2 gate had the lowest LH value, while the NOR-4 gate had the lowest HL value. This underscores how each gate type influences transition time, with more

complex gates like the AOI having longer signal transition times. Conversely, simpler gates, such as the NOR-4 gate, experience less degradation. Similarly, other simpler gates are more consistent in terms of degradation, exhibiting less variation and lower standard deviations compared to more complex gates.

B. SET and SET + Aging effects

In Table IV, the numerical representation of the reduction in critical charge needed to cause a SET is provided, comparing the value of SET Fresh with SET with BTI, as per Equation 3. Analyzing the table, it is evident that different logic gates exhibit varying levels of degradation due to BTI.

For instance, some gates, such as AOI-V2, exhibit lower variation (with a maximum of 8.91% and a standard deviation of 0.55%), indicating more consistent degradation compared to other gates like NAND-4, which has a higher standard deviation (2.34%). The AOI-V2 gate also has the lowest average degradation, suggesting it is more robust against BTI compared to other gates in the table. On the other hand, the NAND-2 gate has a relatively high average degradation (10.26%) and a high standard deviation (1.97%), indicating it may be more susceptible to BTI.

The NOR-3 and AOI-V2 gates appear to be the most robust in terms of average degradation and consistency, while the NAND-4 gate shows the greatest variability, suggesting it may be less reliable under aging conditions. Additionally, it is evident that the average value in the fresh state is 8.91% higher than the value for BTI with SET, demonstrating that cell degradation significantly impacts their robustness.

TABLE IV
REDUCTION IN CRITICAL CHARGE FOR BTI WITH SET RELATIVE TO FRESH SET

	Maximum	Minimum	Mean	Standard Deviation
Inverter	9.52%	8.33%	8.93%	0.84%
NAND-2	12.50%	10.20%	10.26%	1.97%
NAND-3	9.66%	7.14%	8.67%	0.89%
NAND-4	15.38%	4.08%	9.03%	2.34%
NOR-2	11.11%	6.35%	9.05%	1.97%
NOR-3	10.00%	7.69%	8.73%	0.76%
NOR-4	11.76%	4.76%	8.86%	1.56%
AOI-V1	11.11%	7.14%	8.25%	1.27%
AOI-V2	8.91%	7.14%	7.81%	0.55%
OAI-V1	10.26%	7.41%	9.90%	0.92%
OAI-V2	10.34%	7.89%	8.83%	1.05%

V. CONCLUSION

This initial study examines the impacts of radiation on the aging of logic gates, specifically analyzing how logic gates with BTI behave and the likelihood of a SET occurring in them. It is possible that there are synergistic effects between aging and radiation that cannot be predicted through simulations.

The study reveals that aging degradation affects the HL and LH transition times of logic gates. Simpler gates with fewer inputs age more compared to their counterparts with more inputs. The results also show that more complex gates, such as AOI-V1 and AOI-V2, exhibit greater variability in degradation, especially in HL transitions. Notably, the AOI-V2 gate stands out as the most robust against BTI, with the lowest average degradation and the highest consistency, while the NAND-4 gate exhibits the greatest variability, suggesting it may be less reliable under aging conditions.

Comparing BTI with SET effects relative to the fresh state reveals that cell degradation significantly impacts the robustness of logic gates. The average value in the fresh state is 8.91

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